REMARKS

Claim Rejections

35 U.S.C. §103

In the Office Action, claims 1-24 were rejected under 35 U.S.C. 103.

Sample in view of Agrawal

In the Office Action, claims 1-6 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent 6,289,494 to Sample et al. (hereinafter *Sample*) in view of U.S. Patent No. 5,644,496 to Agrawal et al. (hereinafter *Agrawal*) (Examiners Response A). For the reasons stated below Applicants respectfully submit that claims 1-6 are patentable over *Sample* in view of *Agrawal*.

Claim 1 reads:

> A crossbar device comprising:
> n input lines;
> m output lines; and
> a plurality of chains of pass transistors, each chain having a plurality of pass transistors, to selectively couple said n input lines to said m output lines;
> where n and m are integers.

In contrast, *Sample* discloses multiplexer type, crosspoint type and hybrid crosspoint/multiplexer type crossbars. One of these hybrid structures is the prior art implementation discussed in Figure 2 of the present application. In this architecture, multiplexer **630** of Figure 13D drives a crossbar **650**. As stated by the examiner, *Sample* does not disclose placing a pass transistor at the input port of each input line to control inputting data into the multiplexer.

The Examiner cites *Agrawal* for teaching, in Figure 6A, the placement of a pass transistor, via PIP **521**, at the **input port** of a crossbar device (UMP **501**). Applicants respectfully disagree with such a characterization of *Agrawal*. PIP **521** cannot be said to be at the input port of a crossbar device (UMP **501**).

As discussed in the specification of the present invention, the structure disclosed advantageously reduces the parasitic capacitance to a small area as shown in FIG. 5 of the present application. As noted in *Agrawal,* PIP **521** is separated from the MIP connecting PIP 521 to UPM **501** by long line (LL) **520**. As discussed in the background section of *Agrawal*, longlines are longhaul conductor signal routing paths. Thus, by the nature of being separated from UPM **501** by longhaul conductor signal routing path, the PIP **521** cannot be said to be "at the input port of a multiplexer". Moreover, a long signal routing path is going to have a relatively large capacitance. Thus, the structure in *Agrawal* teaches away from the structure of the present invention by disclosing a long signal routing path between the first transistor (PIP **521)** and the second transistor (UPM **501**) resulting in a large capacitance instead of a small capacitance.

In addition, it would not have been obvious to someone at the time of the present application to combine *Sample* and *Agrawal* as *Agrawal* predated *Sample*. Thus, if it would have been obvious from the structure of *Agrawal* to place pass transistors at the front of a multiplexer, *Sample* would arguably have performed this action in his architectures. Assuming, arguendo, the structure shown in Figure 6A illustrates a pass transistor connected to the input of a multiplexer, the Examiner has used impermissible hindsight in attempting justify the combination of *Sample* and *Agrawal.*

For at least the reasons discussed above, Applicants respectfully submit that claim 1 is patentable over *Sample* in view of *Agrawal*.

Claims 2-6 depend from independent claim 1 incorporating its limitations. Thus, by virtue of at least their dependency on claim 1, claims 2-6 also recite patentable subject matter.

Sample in view of Patel and Admitted Prior Art

In the Office Action, claims 7, 13 and 14 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art and U.S. Patent No. 6,175,952 to Patel et al. (hereinafter *Patel*). For the reasons stated below Applicants respectfully submit that claims 7, 13 and 14 are patentable over *Sample* in view of *Patel* and admitted prior art.

Claim 7 reads:

> A reconfigurable circuit comprising:
>
> a plurality of crossbar devices coupled to one another, each crossbar device having at least a memory element, and an output buffer electrically associated with the memory element; and
>
> a voltage supply structure coupled to the crossbar device designed to supply Vdd to the output buffers, and a voltage raised by a threshold over Vdd to the memory elements to maintain the input voltage of the output buffers at Vdd.

Sample and the admitted prior art does not teach a voltage supply structure as recited in the claim 7.

In *Patel*, the disclosure in Figure 23 illustrates the use of separate supply voltage in isolation device **2315** to **protect circuitry connected to the output of isolation**

device 2315. The protected circuitry uses VCC1. The isolation device uses VCC2. The isolation device is intended to prevent high voltages from damaging downstream circuitry **2310** that would otherwise be driven by the signal driving the isolation device **2321** (column 26, lines 39-42). Thus, in *Patel,* the circuitry is designed to prevent higher voltages from being passed to the second stage. In other words, *Patel* is designed to **step down voltages** to protect circuitry in the event the input voltages are above a maximum level. That maximum level is the VCC2 plus the threshold level of device **2320**.

In contrast, the voltage supply structure presently disclosed is designed to provide a higher voltage (e.g. stepped up) at the input to the output buffer. That is, the supply voltage provided to the memory elements is raised by a threshold over Vdd in order to provide input voltages at the input of the output buffer that are at Vdd. There is no discussion in *Patel* relating to a voltage raised by a threshold over Vdd to the memory elements **to maintain the input voltage of the output buffers at Vdd**.

Thus, Applicants respectfully submit that claim 7 is patentable over *Sample* in view of *Patel* and admitted prior art.

Claims 13-14 depend from independent claim 7 incorporating its limitations. Thus, by virtue of at least their dependency on claim 7, claims 13-14 also recite patentable subject matter.

Sample in view of Patel, Agrawal and Admitted Prior Art

In the Office Action, claims 8-12 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art, *Patel* and *Agrawal*. For the reasons stated below Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of *Patel, Agrawal* and admitted prior art.

Claims 8-12 depend from claim 7. In addition to the limitations of claim 7, these claims contain additional limitations substantially similar to claim 1. *Patel* does not solve the deficiencies of the previous arguments with respect to claim 1. In addition, *Agrawal* does not solve the deficiencies of the previous arguments with respect to claim 7. Thus, for at least the reasons set forth with respect to both claim 1 and claim 7 above, Applicants respectfully submit that claims 8-12 are patentable over *Sample* in view of admitted prior art, *Patel* and *Agarwal*.

Sample in view of Burstein and Admitted Prior Art

In the Office Action, claims 15, 16, 23 and 24 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of Applicants' admitted prior art and U.S. Patent No. 5,744,990 to Burstein (hereinafter *Burstein)*. For the reasons stated below, Applicants respectfully submit that claims 15, 16, 23 and 24 are patentable over *Sample* in view of *Burstein* and admitted prior art.

Claim 15, as amended, reads:

> A reconfigurable circuit comprising:
> a plurality of crossbar devices coupled to one another, each crossbar device having at least an output buffer; and

a power-on circuitry coupled to the crossbar devices to force the output buffers to a same known logic value at power-on, said same known logic value to facilitate reduction in current drain by reducing contention on outputs of said plurality of output buffers .

Thus, in the present invention, the output buffers of a crossbar device are forced to a known logic value during power on. The benefit of such forcing to a known logic value is to prevent large current draws since the outputs of the crossbar devices may be coupled together, depending on the device's configuration coming out of reset. Coupled outputs with different output values may result in large current drain in the device and, additionally result in potentially damaging the device. In contrast, *Burstein*, and traditional Power-on-Reset (POR) usage, are concerned with the setting of sequential and clocking devices to known states to provide predictability in the function of such circuits upon recovery from reset. *Burstein* does not discuss contention on the output of devices as they come out of reset.

In addition, there is no motivation to combine the POR circuitry of *Burstein* in a crossbar device of *Sample*. There is no disclosure or suggestion in *Burstein* to use the POR circuitry in a crossbar circuit to prevent large current draws and, resultantly, to prevent potential damage to the crossbar device. Absent some motivation to combine the references, a rejection based on a combination of references is improper.

Thus, for at least the reasons discussed above, Applicants respectfully submit that claim 15 is patentable over *Sample* in view of the admitted prior art and *Burstein*. Claims 16, 22 and 23 depend from claim 15. Thus, for at least the reasons discussed

above with respect to claim 15, Applicants respectfully submit that claims 16, 22 and 23 are patentable over *Sample* in view of the admitted prior art and *Burstein*.

Sample in view of Agrawal, Burstein and Admitted Prior Art

In the Office Action, claims 17-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of *Agrawal*, *Burstein* and Applicants' admitted prior art. For the reasons stated below, Applicants respectfully submit that claims 17-21 are patentable over *Sample* in view of *Agrawal*, *Burstein*, and Applicants' admitted prior art.

Claims 17-21 depend from claim 15. In addition to the limitations of claim 15, these claims contain additional limitations substantially similar to claim 1. *Burstein* does not solve the deficiencies of the previous arguments with respect to claim 1. In addition, *Agrawal* does not solve the deficiencies of the previous arguments with respect to claim 15. *Thus*, Applicants respectfully submit that, for at least the same reasons discussed above with respect to both claims 1 and 15, claims 17-21 are patentable over *Sample* in view of *Agrawal*, *Burstein* and Applicants' admitted prior art.

Sample in view of Burstein, Patel and Admitted Prior Art

In the Office Action, claim 22 was rejected under 35 U.S.C. §103(a) as being unpatentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art. For the reasons stated below, Applicants respectfully submit that claim 22 is patentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art.

Claim 22 depends from claim 15. In addition to the limitations of claim 15, claim 22 contain additional limitations substantially similar to claim 7. *Burstein* does not solve the deficiencies of the previous arguments with respect to claim 7. In addition, *Patel* does not solve the deficiencies of the previous arguments with respect to claim 15. Thus, Applicants respectfully submit that, for at least the same reasons discussed above with respect to both claims 15 and 7, claim 22 is patentable over *Sample* in view of *Burstein*, *Patel* and Applicants' admitted prior art.

Conclusion

In view of the forgoing, Applicants respectfully submit that claims 1-25 are in condition for allowance. Early issuance of the Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge shortages or credit overpayments to Deposit Account No. 500393. A Fee Transmittal is enclosed in duplicate for fee processing purposes.

Respectfully submitted,
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